SHTxx
Humidity & Temperature
Sensmitter

Application Note
ESD, Latch-Up and EMC

1 Introduction

The SHTxx devices are qualified with respect to ESD (Electrostatic Discharge) and Latchup compliant with JESD 22 – A114, MIL Std 883E and JEDEC78 Std. This means the SHTxx device provides excellent protection against these phenomena.
Due to its micro-integration and digital interfacing supported by a CRC checksum, the SHTxx exhibits superior functional immunity against electromagnetic immission (EMI) originated by. e.g. cellular phones, machinery and other RF radiating devices.
This application note elaborates on ESD and Latchup and provides an insight into the protection circuits of the SHTxx device. In case improved ESD protection is required an example of additional external ESD protection is suggested. In addition, information about electromagnetic compatible (EMC) design with the SHTxx device is given.

2 ESD

Electrostatic discharge (ESD) constitute a danger for integrated circuits and therefore, also for the SHTxx device. To cope with this problem the SHTxx device provides state of the art built-in ESD protection circuits on all pins. Functional schematics of ESD protection circuits are given in Fig. 1.

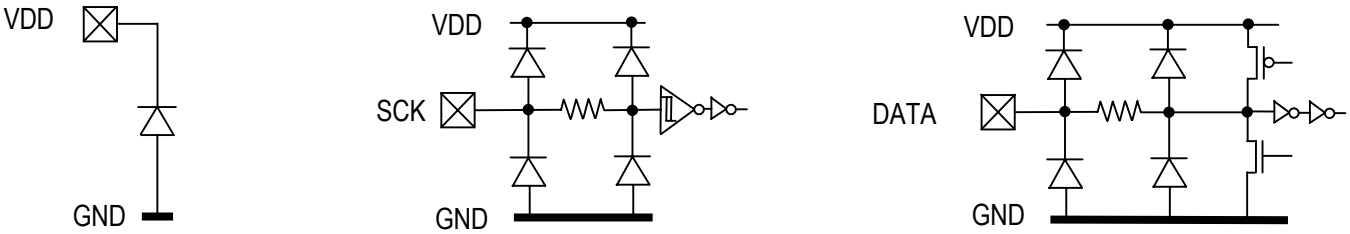

Figure 1 Functional schematic of ESD protection circuits inside the SHTxx.

The SHTxx devices are tested using Human Body Model at 2kV (according to JESD 22 – A114, MIL Std 883E). The test circuit and waveforms are shown in Figure 2.

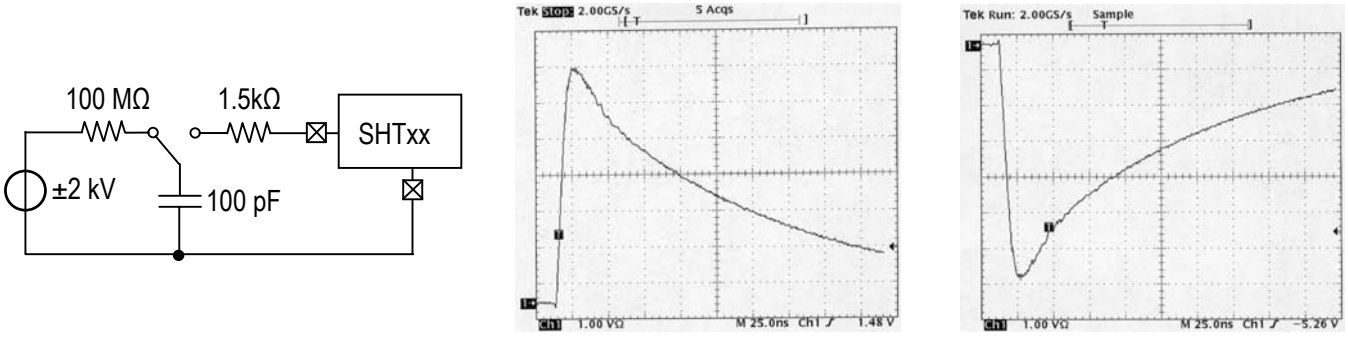

Figure 2 Human-Body Model Test Circuit. The 100pF capacitor simulates the capacitance of the human body, the 1.5 kΩ value of the discharge resistor the internal resistance of the human body.

ESD stress test was performed using a TMT Verifier II s/n 1042049 equipment according to table below:

Stress Level	Stressed Pin	Reference	Polarity
2 kV	SCK	GND	3 positive pulses then 3 negative pulses
	DATA	GND	
	SCK	VDD	
	DATA	VDD	
	GND	VDD	
	SCK	DATA	

Table 1 summarizes the tested configurations of the SHxx device

The SHTxx passes the described Human-Body Model Test. Further details about the ESD test of SHTxx can be found in [Pluto1] (Report available on request at SENSIRION). No further test with higher voltages and other models (such as Machine Model, Charged Device Model, or Charged-Cable Model) have been performed to date. If more stringent specifications are required please contact SENSIRION for the latest status on the SHTxx ESD qualification. Passing the Human-Body Model test according to the described standards means that the SHTxx is well protected against ESD if normal precautions are taken when handling the device.

In case extreme discharge protection is required an additional protection circuit according to Figure 3 can be implemented.

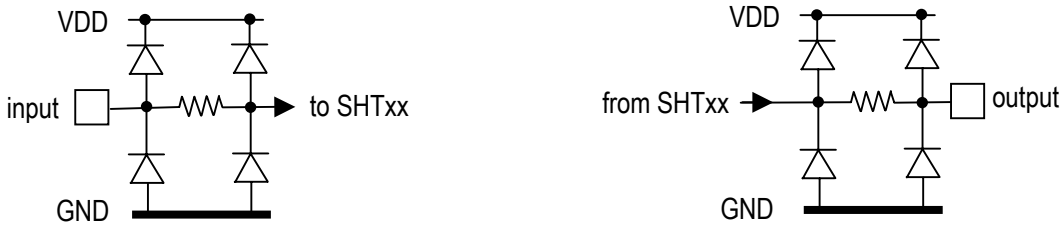

Figure 3 Additional external Protection circuits for SHTxx device (only necessary when the device has to be protected against extreme electrostatic energy, above 100 µWs)

3 Latchup

Isolation of the individual diodes, transistors and capacitors from each other in an integrated cuircuit, such as the SHTxx, is achieved by reverse-biased PN junctions. These junctions form NPN and PNP structures with adjacient junctions which result in parasitic thyristors. These parasitic thyristors may be undesirably triggered in various ways [TI2000].

1. If there is a voltage at the input or output of the SHTxx which is more positive than the supply or more negative than the ground connection current flows into the gate of the parasitic thyristor. If the amplitude and duration of the current are sufficient the thyristor is triggered. With lines of several meters in length and overshoots the probability that the thyristor might be triggered must be taken into account.
2. An electrostatic discharge can trigger the parasitic thyristor. Even if the electrostatic discharges have a duration of only a few tens of nanoseconds the complete chip may be flooded with charge carries, which then flow away slowly, resulting in the triggering of the thyristor.
3. The parasitic thyristor may be triggered by a high supply voltage - far higher than the value given in data sheet.

Although these conditions violate the specifications given in the SHTxx data sheet they may occur during uncontrolled events during operation. The SHTxx device was designed obeying state-of-the art precautions to reduce the thyristors sensitivity to the maximum thus to avoid latch-up in all above mentioned situations.
In order to verify the latch-up immunity the SHTxx device are tested according to JEDEC Std 78. Figure 4 shows the test setup. The test was performed at 85°C using a ORYX 11000EX test system.

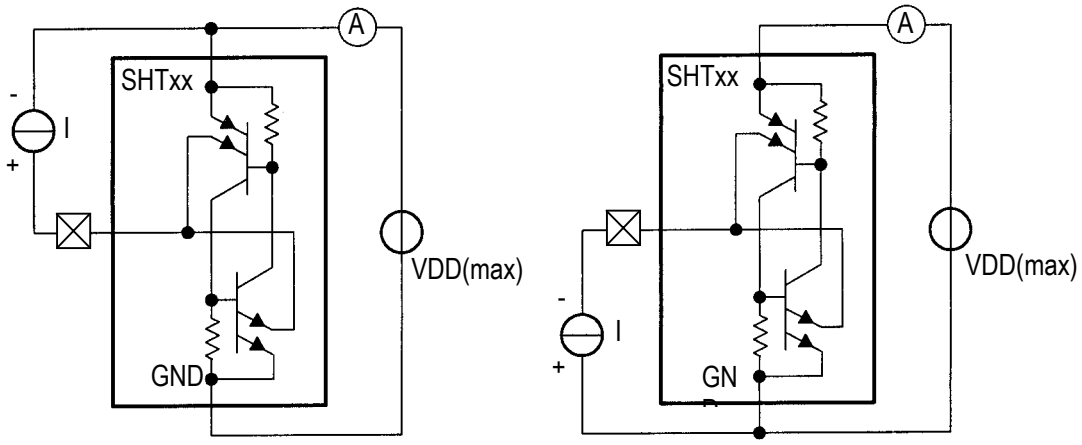

Figure 4 Latchup test setup. The SHTxx is modeled here as a parasitic thyristor.

A current *I* of ±100mA is injected with VDD(max) of 9V compliance. After this trigger impulse the supply current *A* is measured and compared to the current measured before the latchup trigger was applied. If no current difference is observed and functionality of the device is verified the test is passed. The test is performed on all pins of the SHTxx. A detailed report is given in [Pluto2] (Report available on request at SENSIRION).

4 EMC

The SHTxx devices are exceptionally well suited to retain reliable functionality in demanding environments. Advantages are listed below:

1. No external components (except the pull up resistor on the DATA line) are required. All susceptible circuit is integrated at micrometer scale making it inherently immune against RF radiation (originated by wireless devices).
2. The pure digital interfacing to the SHTxx devices allows low S/N ratio on the SCK and DATA lines.
3. The transmission frequency of the measurement data through the SCK and DATA lines can be set arbitrarily low hence the slopes of the signals can be filtered to minimize susceptibility against bursts.
4. The CRC (cyclic redundancy check) allows the user to verify whether the transfer of the data has been performed properly. For more details refer to [CRC].

SENSIRION recommends the following basic precautions when designing with the SHT11 device:

1. Using a capacitor between VDD and GND as close as possible to the SHTxx pins
2. Avoid running the SCK and DATA lines next to each other when using a long ribbon cable or flat flexible cable to minimize cross talk.
3. Reduce transmission frequency and slopes of the signals when using long cables. This is to reduce cross talk sensitivity, reflections and susceptibility against bursts. Slopes can be reduced by inserting a passive low pass filter, shown in Fig. 5. Best results may be achieved when using a low pass filter on either side of the cable connection.

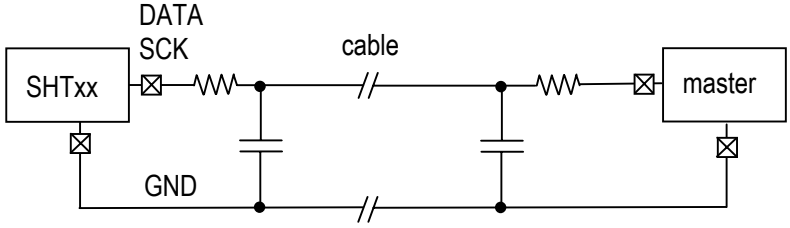

Figure 5 Reducing the slope of SCK of DATA line when using a long cable with the SHTxx device.

5 References

[Pluto1] Serma Technologies, "ESD Experiment on PLUTO", Sensirion Qualification Report, Sept 2001.
[TI2000] Eilhard Haseloff, Texas Instruments, "Latch-Up, ESD, and Other Phenomena", Application Report May 2000.
[Pluto2] Serma Technologies, "Latch-up Experiment PLUTO", Sensirion Qualification Report, Sept 2001.
[CRC] Sensirion, "Application Note CRC", Sensirion Application Note, 2002.

6 Revision history

Date	Revision	Changes
May 6, 2002	0.9 (Preliminary)	Initial revision
Oct. 17, 2003	1.0 (Preliminary)	Changed download link
May 25, 2005	1.1	Changed company address
Oct. 3, 2006	1.2	Sensirion Inc. address added

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